Atty. Dkt. No. 39153/433 (C167596-CIP)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sander, et al.

Title: MINIMIZING TRANSISTOR SIZE IN INTEGRATED CIRCUITS

Appl. No.: unknown

Filing Date: unknown

Examiner: Nguyen, T.

Art Unit: 2813

CERTIFICATE OF EXPRESS MAILING

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Karen Meier (Printed Name)

Karen Klein (Signature)

PRELIMINARY AMENDMENT

Commissioner for Patents
Box CPA
Washington, D.C. 20231

Sir:

Please amend the application as follows:

IN THE SPECIFICATION:

On page 1, delete the first full paragraph, and replace this paragraph with the following in accordance with 37 C.F.R. §1.121. A marked up version showing changes is attached.

The present application is a divisional of U.S. Application No. 09/515,875 filed on February 29, 2000 by Sander, et al. which is a continuation-in-part application of U.S. Application No. 09/119,934 filed on July 21, 1998 by Klein, et al.

IN THE CLAIMS:

Please cancel claims 1-18 without prejudice.

Please add new claims 23-38.

23. (New) The method of claim 21, wherein the insulating liners are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

24. (New) The method of claim 21, wherein a source and drain are disposed by at least partially beneath the insulating liners.

25. (New) An integrated circuit including at least a pair of local interconnects with one interconnect on each side of a gate of a transistor, the integrated circuit being manufactured by a method comprising steps of:

forming on a semiconductor substrate a thick insulating layer;

forming at least a pair of spaced apart openings in the insulating layer adjacent the semiconductor substrate;

forming a source in one of the openings and a drain in the other of the openings;

filling each of the openings with a conductive material to form the local interconnects, the local interconnects being electrically coupled to the source and drain;

removing a portion of the insulating layer to form a gate opening between the local interconnects;

forming a gate dielectric on the semiconductor substrate in the gate opening; and

forming the gate on the gate dielectric in the gate opening between the local interconnects.

26. (New) The integrated circuit of Claim 25, wherein the space between the pair of openings is one minimum photolithographic feature and the local interconnects are each one minimum photolithographic feature.

27. (New) The integrated circuit of Claim 25, wherein insulating spacers are each disposed on an interconnect wall adjacent the gate to separate each of the local interconnects from the gate.

28. (New) The integrated circuit of Claim 25, wherein the source and drain are formed by implanting impurities in the pair of openings in the insulating layer.

29. (New) The integrated circuit of Claim 25, wherein the portion of insulating layer removed to form the gate opening is removed by using a masking material with an opening in the masking material positioned between the pair of local interconnects.

30. (New) The integrated circuit of Claim 29, wherein the opening in the masking material extends over but not beyond each of the pair of local interconnects.

31. (New) The integrated circuit of Claim 30, wherein the opening in the masking material is positioned over an active region in the semiconductor substrate, the active region being surrounded by an isolation region, the opening in the masking material extending to or beyond the active region.

32. (New) The integrated circuit of Claim 25, wherein a conductive layer is formed on walls of the to line the spaced apart openings and a remainder of the spaced apart openings are filled with another conductive material.

33. (New) The integrated circuit of Claim 25, wherein the conductive layer is polysilicon and the another conductive material is tungsten.

34. (New) The integrated circuit of Claim 33, wherein the polysilicon is the origin for the impurities for the source and drain.

35. (New) The integrated circuit of Claim 25, wherein a barrier layer is formed on the walls of the spaced apart openings to line the opening and a remainder of the local interconnect opening is filled with a conductive material.

36. (New) The integrated circuit of Claim 35, wherein the barrier layer includes titanium nitride.

37. (New) The integrated circuit of Claim 25, wherein an insulating etch stop layer is formed on semiconductor substrate before forming the thick insulating layer.

38. (New) The integrated circuit of Claim 37, wherein the etch selectivity of the etch stop layer is different from the etch selectivity of the insulating layer.

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

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Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested. The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 4-30-01

By _____

Joseph N. Ziebert
Attorney for Applicant
Registration No. 35,421

FOLEY & LARDNER
Firstar Center
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5367
Telephone: (414) 297-5768
Facsimile: (414) 297-4900

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

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